AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains either a strikethrough ("——") or is enclosed by double brackets ("[[ ]]").

LISTING OF CLAIMS

1-7. (Canceled)

8. (Original) A method of accessing Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM) memory storage employed in a packet switch, the DDR SDRAM memory having a plurality of memory banks for storing packet data of a plurality of packets, the method comprising steps of:

a. segmenting packet data into variable size burst units;

b. sequencing a plurality of burst unit memory write operations ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation;

c. sequencing a plurality of burst unit memory read operations ensuring that each bust unit memory read operation reads packet data from a memory bank different from the previous burst unit memory read operation;

d. arranging the plurality of sequenced burst unit memory write operations in a plurality of write windows;

e. arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows; and

f. performing memory access operations interleaving the write windows with the

read windows.

9. (Original) The method claimed in claim 8, wherein segmenting packet data into variable size burst units, the method further comprises a step of:

segmenting packet data in respect of packets received via a plurality of input switch ports prior to storing the packet data into the memory storage.

10. (Original) The method claimed in claim 9, further comprising a prior step of: enforcing packet acceptance control.

11. (Original) The method claimed in claim 10, wherein enforcing packet acceptance control, the method further comprises a step from: selectively accepting a packet, and selectively discarding another packet.

12. (Original) The method claimed in claim 9, wherein sequencing the plurality of memory burst unit memory write operations, the method further comprises a step of:

preferentially scheduling write burst units corresponding to a packet from one of:

a packet received via a high bandwidth input port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet.

13. (Original) The method claimed in claim 12, wherein preferentially scheduling write burst units, the method further comprises a step of:

delaying scheduling of write burst units totaling less than ten memory access cycles long to a single bank.

14. (Original) The method claimed in claim 8, wherein segmenting packet data into variable size burst units, the method further comprises segmenting packet data in respect of packets stored in the memory storage for transmission via a plurality of output switch ports.

15. (Original) The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of:

preferentially scheduling read burst units corresponding to packets from one of:

a packet to be transmitted via a high bandwidth output port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet.

16. (Original) The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of:

delaying scheduling of read burst units corresponding to packets destined to a congested output port.

17. (Original) The method claimed in claim 14, wherein sequencing the plurality of memory burst unit memory read operations, the method further comprises a step of:

delaying scheduling of read burst units totaling less than ten memory access cycles long to a single bank.

18. (Original) The method claimed in claim 8, wherein segmenting packet data, the method further comprises a step of: segmenting packet data into at least four memory access cycles long burst units.

19. (Original) The method claimed in claim 18, wherein segmenting packet data, the method further comprises a step of: segmenting packet data into burst units transferring at least 49 bytes of packet data.

20. (Original) The method claimed in claim 8, further employing windows at least 128 memory access cycles long.

21. (New) A method comprising:

segmenting packet data into variable size burst units based on a predefined rule;

sequencing a plurality of memory write operations such that each memory write operation writes packet data to a memory bank different from the previous memory write operation;

sequencing a plurality of burst unit memory read operations such that each memory read operation reads packet data from a memory bank different from the previous memory read operation;

arranging the plurality of sequenced burst unit memory write operations in a plurality of write windows;

arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows, wherein the windows are at least a predetermined minimum size; and

performing memory access operations by interleaving the write windows with the read windows.

22. (New) The method of claim 21, wherein segmenting packet data into variable size burst units based on a predefined rule comprises segmenting packet data such that the burst units are between a predetermined minimum and a predetermined maximum burst unit size.

23. (New) The method of claim 22, wherein segmenting packet data into variable size burst units based on a predefined rule further comprises segmenting packet data such that the burst units have a predetermined median burst unit size.

24. (New) The method of claim 21, wherein the predetermined minimum size is 128 memory access cycles.

25. (New) A system comprising:

means for partitioning packet data, wherein the partitioned packet data size falls between a predetermined minimum and a predetermined maximum burst unit size;

means for arranging burst unit memory write operations, wherein each memory write operation writes packet data to a memory bank different from the previous memory write operation;

means for arranging burst unit memory read operations, wherein each memory read operation reads packet data from a memory bank different from the previous memory read operation;

means for arranging the burst unit memory write operations in a plurality of write windows;

means for arranging the burst unit memory read operations in a plurality of read windows; and

means for interleaving the write windows with the read windows to perform memory access operations.

26. (New) The system of claim 25, wherein the windows are at least 128 memory access cycles long.

27. (New) The system of claim 25, wherein the predetermined minimum burst unit size is 49 bytes of packet data.